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sgmii serial interface designed for high speed communication functions as a serial interface transmitting data sequentially fewer pins space efficient and compatible with various phy devices rgmii rgmii is a reduced pin count variant of gmii cuts pin count versus original gmii for smaller board designs fundamentally the mii sgmii rgmii signals are for data that a mac device converts to phy phy is the physical media you attach to cat5 6 cable or fiber or wifi thus for each ethernet supported device you will have either sgmii rgmii interfaces for the data stream rgmii version 1 3 uses 2 5v cmos whereas rgmii version 2 uses 1 5v hstl serial gigabit media independent interface the serial gigabit media independent interface sgmii is a variant of mii used for gigabit ethernet but can also carry 10 100 mbit s ethernet sgmii using low voltage differential signaling lvds offers the benefit of 10x the data bandwidth with fewer signal lines shrinking solution size rgmii still uses single ended signaling but again offers a 10x increase in data bandwidth for only 3 additional signal lines compared to rmii there are phys with rgmii sgmii and mdi in these case rgmii connect to mac sgmii connect to a media module such as sfp module which can be fiber or copper mdi as usual for copper transformer interface in some phy the link to mac is over sgmii the serial gigabit media independent interface sgmii is designed to satisfy the following requirements convey network data and port speed between a 10 100 1000 phy and a mac with significantly less signal pins than required for gmii operate in both half and full duplex and at all port speeds the 100mbps versions of the mii 15 pin mii and nine pin reduced mii rmii are complemented by 1gbps versions which include reduced gigabit mii rgmii and serial gigabit mii sgmii rgmii is a 12 pin interface while sgmii can operate as either a four or six pin interface the serial gigabit media independent interface sgmii is a popular gigabit ethernet phy interface and it holds various advantages over both gmii and rgmii this article reviews some of the core sgmii concepts with the help of a scope and lab bench examples updated sep 28 2023 overview rmii and rgmii phy interfaces an 886 intel agilex device design guidelines download pdf view more a newer version of this document is available customers should click here to go to the newest version document table of contents x 1 introduction to the intel agilex device design guidelines 2 system specification 3 device selection 4 rgmii 10 100 1000 mbit s 4 bit 12 125 mhz 1 8 2 5 3 3 5v sgmii 10 100 1000 mbit s 1 lane 4 625 mhz speed data width pin count clock frequency voltage level speed data width pin count clock frequency standard xmii variants for automotive today incompatibility conflicting requirements different pads level translators add cost delays agenda review past mii solutions parallel buses mii rmii gmii rgmii command space in parallel buses serial buses smii sgmii multi port serial buses qsgmii usgmii 10g mgig mii xgmii usxgmii mp usxgmii path forward proposal leveraged solution for multi port and single port 10 100 hd fd spe motivation 802 3dg wants a new mii 1 answer sorted by 1 on q1 what you ve shown for the driver is just one case the one where voh is at it s max and vol is at it s minimum which will never occur at the same time the 650 mv output differential voltage you show from that case is greater than the max output differential voltage specification of 400 mv figure 1 mac to ethernet phy rgmii interface the txv0106 and txv0108 are one of the first translator devices to support rgmii interface signaling specifications with rgmii friendly pin outs enabling system designers to easily implement rgmii level translation as well as translation for other skew sensitive interfaces rgmii reduced gigabit media independent interface sgmii serial gigabit media independent interface 2 1 mii 10 100m interface in mii mode there are 16 signals as shown in the picture below plus two other ones for mdio and mdc in this mode both txclk and rxclk provided by phy clock rate is 2 5 mhz for 10mbps and 25mhz for 100mbps get an rgmii processor to link to an sgmii based ethernet switch this document will cover various design considerations for connecting an embedded microprocessor with a gmii or rgmii mac interface to an sgmii based gigabit ethernet switch this document will address system hardware and software sgmii is a serial interface for gigabit ethernet that replaces previous standards like gmii and rgmii this interface requires fewer physical pins so it simplifies hardware routing and layout one external mac port with sgmii one external mac port with rgmii mii rmii rgmii v2 0 rmii v1 2 with 50mhz reference clock input output option mii in phy mac mode five integrated phy ports 1000base t 100base tx 10base te ieee 802 3 fast link up option significantly reduces link up time auto negotiation and auto mdi mdi x the rgmii interface is a dual data rate ddr interface that consists of a transmit path from fpga to phy and a receive path from phy to fpga both paths have an independent clock 4 data signals and a control signal rgmii and sgmii 10base te 100base tx 1000base t 100base fx and 1000base x are supported on the media interface the dp83869hm can support several unique modes of operation 5 rk3568□□□qsgmii□□ □□ rgmii□□rk3588 rk3568□sgmii qsgmii □□□□□□□□□□□ □□□□□□□□ rk3568□sgmii qsgmii □□□□□□□□□□□ □□□□□□□□ □□□□□ 207 □□□ 0 □□□ 9 □□□□□ 0 □□□□ 10 □□□□ 0 □□□□

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sgmii serial interface designed for high speed communication functions as a serial interface transmitting data sequentially fewer pins space efficient and compatible with various phy devices rgmii rgmii is a reduced pin count variant of gmii cuts pin count versus original gmii for smaller board designs

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fundamentally the mii sgmii rgmii signals are for data that a mac device converts to phy phy is the physical media you attach to cat5 6 cable or fiber or wifi thus for each ethernet supported device you will have either sgmii rgmii interfaces for the data stream

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sgmii using low voltage differential signaling lvds offers the benefit of 10x the data bandwidth with fewer signal lines shrinking solution size rgmii still uses single ended signaling but again offers a 10x increase in data bandwidth for only 3 additional signal lines compared to rmii

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there are phys with rgmii sgmii and mdi in these case rgmii connect to mac sgmii connect to a media module such as sfp module which can be fiber or copper mdi as usual for copper transformer interface in some phy the link to mac is over sgmii

serial gmii specification archive org Oct 24 2023

the serial gigabit media independent interface sgmii is designed to satisfy the following requirements convey network data and port speed between a 10 100 1000 phy and a mac with significantly less signal pins than required for gmii operate in both half and full duplex and at all port speeds

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the 100mbps versions of the mii 15 pin mii and nine pin reduced mii rmii are complemented by 1gbps versions which include reduced gigabit mii rgmii and serial gigabit mii sgmii rgmii is a 12 pin interface while sgmii can operate as either a four or six pin interface

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the serial gigabit media independent interface sgmii is a popular gigabit ethernet phy interface and it holds various advantages over both gmii and rgmii this article reviews some of the core sgmii concepts with the help of a scope and lab bench examples updated sep 28 2023 overview

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agenda review past mii solutions parallel buses mii rmii gmii rgmii command space in parallel buses serial buses smii sgmii multi port serial buses qsgmii usgmii 10g mgig mii xgmii usxgmii mp usxgmii path forward proposal leveraged solution for multi port and single port 10 100 hd fd spe motivation 802 3dg wants a new mii

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1 answer sorted by 1 on q1 what you ve shown for the driver is just one case the one where voh is at it s max and vol is at it s minimum which will never occur at the same time the 650 mv output differential voltage you show from that case is greater than the max output differential voltage specification of 400 mv

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figure 1 mac to ethernet phy rgmii interface the txv0106 and txv0108 are one of the first translator devices to support rgmii interface signaling specifications with rgmii friendly pin outs enabling system designers to easily implement rgmii level translation as well as translation for other skew sensitive interfaces

network management interfaces stmicroelectronics *Feb 16 2023*

rgmii reduced gigabit media independent interface sgmii serial gigabit media independent interface 2 1 mii 10 100m interface in mii mode there are 16 signals as shown in the picture below plus two other ones for mdio and mdc in this mode both txclk and rxclk provided by phy clock rate is 2 5 mhz for 10mbps and 25mhz for 100mbps

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sgmii is a serial interface for gigabit ethernet that replaces previous standards like gmii and rgmii this interface requires fewer physical pins so it simplifies hardware routing and layout

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one external mac port with sgmii one external mac port with rgmii mii rmii rgmii v2 0 rmii v1 2 with 50mhz reference clock input output option mii in phy mac mode five integrated phy ports 1000base t 100base tx 10base te ieee 802 3 fast link up option significantly reduces link up time auto negotiation and auto mdi mdi x

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the rgmii interface is a dual data rate ddr interface that consists of a transmit path from fpga to phy and a receive path from phy to fpga both paths have an independent clock 4 data signals and a control signal

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rgmii and sgmii 10base te 100base tx 1000base t 100base fx and 1000base x are supported on the media interface the dp83869hm can support several unique modes of operation

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