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Proceedings of First Asian Symposium on Cellular Automata Technology Synthesis of Finite State Machines Information Hiding Foreign Service Regulations of the United States of America Advances in Signal Processing and Communication CAD for Hardware Security Official Gazette of the United States Patent and Trademark Office Proceedings of the Fourth International Network Conference 2004 (INC2004) Cloud Computing and Security Hardware Protection through Obfuscation U-M Computing News Embedded System Design The Compacts of Free Association and legislative hearing on H.R. 2408, H.R. 3407 and H.R. 4938 The Gospel of the Flying Spaghetti Monster Logic Synthesis and Verification Introduction to Hardware Security and Trust Introduction to VLSI Design Flow EDA for IC Implementation, Circuit Design, and Process Technology Fundamentals of IP and SoC Security Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology Foundations of Hardware IP Protection Secure System Design and Trustable Computing Frequency Specific Microcurrent in Pain Management E-book Understanding Logic Locking The Unknown Component Problem High-Capacity Local and Metropolitan Area Networks Field-Programmable Logic and Applications: Reconfigurable Computing Is Going Mainstream Architecting Dependable Systems V Advanced Modeling and Simulation of Nuclear Reactors Software Engineering and Formal Methods Correct Hardware Design and Verification Methods Algorithms for Synthesis and Testing of Asynchronous Circuits Low-Power NoC for High-Performance SoC Design Trends in Network and Communications A Practical Handbook for Software Development Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Compact of Free Association Product-Focused Software Process Improvement VLSI Implementations for Image Communications Emerging Topics in Hardware Security

Proceedings of First Asian Symposium on Cellular Automata Technology

2022-04-27

this book gathers selected research papers presented at the first asian symposium on cellular automata technology ascat 2022 organized online by academicians from kolkata india during march 3 5 2022 the book presents one of the most emergent areas in natural computing cellular automaton ca ca is a paradigm of uniform fine grained parallel computation which has been explored to understand complex systems by developing its model at the microscopic level the book discusses many real life problems in the domain of very large scale integration vlsi design and test pattern recognition and classification cryptography pseudo random pattern generation image processing sensor networks material science etc by using ca

Synthesis of Finite State Machines

2012-12-06

synthesis of finite state machines logic optimization is the second in a set of two monographs devoted to the synthesis of finite state machines fsms the first volume synthesis of finite state machines functional optimization addresses functional optimization whereas this one addresses logic optimization the result of functional optimization is a symbolic description of an fsm which represents a sequential function chosen from a collection of permissible candidates logic optimization is the body of techniques for converting a symbolic description of an fsm into a hardware implementation the mapping of a given symbolic representation into a two valued logic implementation is called state encoding or state assignment and it impacts heavily area speed testability and power consumption of the realized circuit the first part of the book introduces the relevant background presents results previously scattered in the literature on the computational complexity of encoding problems and surveys in depth old and new approaches to encoding in logic synthesis the second part of the book presents two main results about symbolic minimization a new procedure to find minimal two level symbolic covers under face dominance and disjunctive constraints and a unified frame to check encodability of encoding constraints and find codes of minimum length that satisfy them the third part of the book introduces generalized prime implicants gpis which are the counterpart in symbolic minimization of two level logic to prime implicants in two valued two level minimization gpis enable the design of an exact procedure for two level symbolic minimization based on a covering step which is complicated by the need to guarantee encodability of the final cover a new efficient algorithm to verify encodability of a selected cover is presented if a cover is not encodable it is shown how to augment it minimally until an encodable superset of gpis is determined to handle encodability the authors have extended the frame to satisfy encoding constraints presented in the second part the covering problems generated in the minimization of gpis tend to be very large recently large covering problems have been attacked successfully by representing the covering table with binary decision diagrams bdd in the fourth part of the book the authors introduce such techniques and extend them to the case of the implicit minimization of gpis where the encodability and augmentation steps are also performed implicitly synthesis of finite state machines logic optimization will be of interest to researchers and professional engineers who work in the area of computer aided design of integrated circuits

Information Hiding

2004-12-17

this book constitutes the thoroughly refereed post proceedings of the 6th international workshop on information hiding ih 2004 held in toronto canada in august 2004 the 25 revised full papers presented were carefully selected during two rounds of reviewing and revision from 70 papers submitted the papers are organized in topical sections on digital media watermarking steganalysis forensic applications steganography software watermarking security and privacy anonymity and data hiding in unusual content

Foreign Service Regulations of the United States of America

1941

this book is a collection of selected peer reviewed papers presented at the international conference on signal processing and communication icsc 2018 it covers current research and developments in the fields of communications signal processing vlsi circuits and systems and embedded systems the book offers in depth discussions and analyses of latest problems across different sub fields of signal processing and communications the contents of this book will prove to be useful for students researchers and professionals working in electronics and electrical engineering as well as other allied fields

Advances in Signal Processing and Communication

2018-11-19

this book provides an overview of current hardware security problems and highlights how these issues can be efficiently addressed using computer aided design cad tools authors are from cad developers ip developers soc designers as well as soc verification experts readers will gain a comprehensive understanding of soc security vulnerabilities and how to overcome them through an efficient combination of proactive countermeasures and a wide variety of cad solutions

CAD for Hardware Security

2023-05-11

THIS BOOK CONSTITUTES THE PROCEEDINGS OF THE INTERNATIONAL CONFERENCE ON CLOUD COMPUTING AND SECURITY ICCCS 2015 WILL BE HELD ON AUGUST 13 15 2015 IN NANJING CHINA THE OBJECTIVE OF ICCCS 2015 IS TO PROVIDE A FORUM FOR RESEARCHERS ACADEMICIANS ENGINEERS INDUSTRIAL PROFESSIONALS STUDENTS AND GOVERNMENT OFFICIALS INVOLVED IN THE GENERAL AREAS OF INFORMATION SECURITY AND CLOUD COMPUTING

Official Gazette of the United States Patent and Trademark Office

1998

THIS BOOK INTRODUCES READERS TO VARIOUS THREATS FACED DURING DESIGN AND FABRICATION BY TODAY S INTEGRATED CIRCUITS ICS AND SYSTEMS THE AUTHORS DISCUSS KEY ISSUES INCLUDING ILLEGAL MANUFACTURING OF ICS OR IC OVERPRODUCTION INSERTION OF MALICIOUS CIRCUITS REFERRED AS HARDWARE TROJANS WHICH CAUSE IN FIELD CHIP SYSTEM MALFUNCTION AND REVERSE ENGINEERING AND PIRACY OF HARDWARE INTELLECTUAL PROPERTY IP THE AUTHORS PROVIDE A TIMELY DISCUSSION OF THESE THREATS ALONG WITH TECHNIQUES FOR IC PROTECTION BASED ON HARDWARE OBFUSCATION WHICH MAKES REVERSE ENGINEERING AN IC DESIGN INFEASIBLE FOR ADVERSARIES AND UNTRUSTED PARTIES WITH ANY REASONABLE AMOUNT OF RESOURCES THIS EXHAUSTIVE STUDY INCLUDES A REVIEW OF THE HARDWARE OBFUSCATION METHODS DEVELOPED AT EACH LEVEL OF ABSTRACTION RTL GATE AND LAYOUT FOR CONVENTIONAL IC MANUFACTURING NEW FORMS OF OBFUSCATION FOR EMERGING INTEGRATION STRATEGIES SPLIT MANUFACTURING 2 5D ICS AND 3D ICS AND ON CHIP INFRASTRUCTURE NEEDED FOR SECURE EXCHANGE OF OBFUSCATION KEYS ARGUABLY THE MOST CRITICAL ELEMENT OF HARDWARE OBFUSCATION

Proceedings of the Fourth International Network Conference 2004 (INC2004)

2016-01-04

EMBEDDED SYSTEMS AND THE INTERNET OF THINGS ARE CURRENT MAJOR EFFORTS IN INDUSTRY AND WILL CONTINUE TO BE MAINSTREAM COMMERCIAL ACTIVITIES FOR THE FORESEEABLE FUTURE EMBEDDED SYSTEMS DESIGN PRESENTS METHODOLOGIES FOR DESIGNING SUCH SYSTEMS AND DISCUSSES MAJOR ISSUES BOTH PRESENT AND FUTURE THAT DESIGNERS MUST CONSIDER IN BRINGING PRODUCTS WITH EMBEDDED PROCESSING TO THE MARKET IT STARTS FROM THE FIRST STEP AFTER PRODUCT PROPOSAL BEHAVIORAL MODELLING AND CARRIES THROUGH STEPS FOR MODELLING INTERNAL OPERATIONS THE BOOK DISCUSSES METHODS FOR AND ISSUES IN DESIGNING SAFE RELIABLE AND ROBUST EMBEDDED SYSTEMS IT COVERS THE SELECTION OF PROCESSORS AND RELATED HARDWARE AS WELL AS ISSUES INVOLVED IN DESIGNING THE RELATED SOFTWARE FINALLY THE BOOK PRESENT ISSUES THAT WILL OCCUR IN SYSTEMS DESIGNED FOR THE INTERNET OF THINGS THIS BOOK IS FOR JUNIOR SENIOR MS STUDENTS IN COMPUTER SCIENCE COMPUTER ENGINEERING AND ELECTRICAL ENGINEERING WHO INTEND TO TAKE JOBS IN INDUSTRY DESIGNING AND IMPLEMENTING EMBEDDED SYSTEMS AND INTERNET OF THINGS APPLICATIONS FOCUSES ON THE DESIGN OF EMBEDDED SYSTEMS STARTING FROM PRODUCT CONCEPTION THROUGH HIGH LEVEL MODELING AND UP TO THE SELECTION OF HARDWARE SOFTWARE AND NETWORK PLATFORMS DISCUSSES THE TRADE OFFS OF THE VARIOUS TECHNIQUES PRESENTED SO THAT ENGINEERS WILL BE ABLE TO MAKE THE BEST CHOICES FOR DESIGNS FOR FUTURE PRODUCTS CONTAINS A SECTION WITH THREE CHAPTERS ON MAKING DESIGNS THAT ARE RELIABLE ROBUST AND SAFE INCLUDES A DISCUSSION OF THE TWO MAIN MODELS FOR THE STRUCTURE OF THE INTERNET OF THINGS AS WELL AS THE ISSUES ENGINEERS WILL NEED TO TAKE INTO CONSIDERATION IN DESIGNING FUTURE IOT APPLICATIONS USES THE DESIGN OF A BRIDGE CONTROL SYSTEM AS A CONTINUING EXAMPLE ACROSS MOST OF THE CHAPTERS IN ORDER TO ILLUSTRATE THE DIFFERENCES AND TRADE OFFS OF THE VARIOUS TECHNIQUES

Cloud Computing and Security

2017-01-02

CAN I GET A RAMEN FROM THE CONGREGATION BEHOLD THE CHURCH OF THE FLYING SPAGHETTI MONSTER FSM TODAY S FASTEST GROWING CARBOHYDRATE BASED RELIGION ACCORDING TO CHURCH FOUNDER BOBBY HENDERSON THE UNIVERSE AND ALL LIFE WITHIN IT WERE CREATED BY A MYSTICAL AND DIVINE BEING THE FLYING SPAGHETTI MONSTER WHAT DRIVES THE FSM S DEVOUT FOLLOWERS A K A PASTAFARIANS SOME SAY IT S THE ASSURING TOUCH FROM THE FSM S NOODLY APPENDAGE THEN THERE ARE THOSE WHO LOVE THE WORSHIP SERVICE WHICH IS CONDUCTED IN PIRATE TALK AND ATTENDED BY CONGREGANTS IN DASHING BUCCANEER GARB STILL OTHERS ARE DRAWN TO THE CHURCH S FLIMSY MORAL STANDARDS RELIGIOUS HOLIDAYS EVERY FRIDAY OR THE FACT THAT PASTAFARIAN HEAVEN IS WAY COOLER DOES YOUR HEAVEN HAVE A STRIPPER FACTORY AND A BEER VOLCANO INTELLIGENT DESIGN HAS FINALLY MET ITS MATCH AND IT HAS NOTHING TO DO WITH APES OR THE OLIVE GARDEN OF EDEN WITHIN THESE PAGES BOBBY HENDERSON OUTLINES THE TRUE FACTS DISPELLING SUCH MALICIOUS MYTHS AS EVOLUTION ONLY A THEORY SCIENCE ONLY A LOT OF THEORIES AND WHETHER WE RE REALLY DESCENDED FROM APES FACT HUMANS SHARE 95 PERCENT OF THEIR DNA WITH CHIMPANZEES BUT THEY SHARE 99 9 PERCENT WITH PIRATES SEE WHAT IMPRESSIVELY CREDENTIALED TOP SCIENTISTS HAVE TO SAY IF INTELLIGENT DESIGN IS TAUGHT IN SCHOOLS EQUAL TIME SHOULD BE GIVEN TO THE FSM THEORY AND THE NON FSM THEORY PROFESSOR DOUGLAS SHAW PH D DO NOT BE HYPOCRITICAL ALLOW EQUAL TIME FOR OTHER ALTERNATIVE THEORIES LIKE FSMISM WHICH IS BY FAR THE TASTIER CHOICE J SIMON PH D IN MY SCIENTIFIC OPINION WHEN COMPARING THE TWO THEORIES FSM THEORY SEEMS TO BE MORE VALID THAN CLASSIC ID THEORY AFSHIN BEHESHTI PH D READ THE BOOK AND DECIDE FOR YOURSELF

Hardware Protection through Obfuscation

1988

RESEARCH AND DEVELOPMENT OF LOGIC SYNTHESIS AND VERIFICATION HAVE MATURED CONSIDERABLY OVER THE PAST TWO DECADES MANY COMMERCIAL PRODUCTS ARE AVAILABLE AND THEY HAVE BEEN CRITICAL IN HARNESSING ADVANCES IN FABRICATION TECHNOLOGY TO PRODUCE TODAY S PLETHORA OF ELECTRONIC COMPONENTS WHILE THIS MATURITY IS ASSURING THE ADVANCES IN FABRICATION CONTINUE TO SEEMINGLY PRESENT UNWIELDY CHALLENGES LOGIC SYNTHESIS AND VERIFICATION PROVIDES A STATE OF THE ART VIEW OF LOGIC SYNTHESIS AND

VERIFICATION IT CONSISTS OF FIFTEEN CHAPTERS EACH FOCUSING ON A DISTINCT ASPECT EACH CHAPTER PRESENTS KEY DEVELOPMENTS OUTLINES FUTURE CHALLENGES AND LISTS ESSENTIAL REFERENCES TWO UNIQUE FEATURES OF THIS BOOK ARE TECHNICAL STRENGTH AND COMPREHENSIVENESS THE BOOK CHAPTERS ARE WRITTEN BY TWENTY EIGHT RECOGNIZED LEADERS IN THE FIELD AND REVIEWED BY EQUALLY QUALIFIED EXPERTS THE TOPICS COLLECTIVELY SPAN THE FIELD LOGIC SYNTHESIS AND VERIFICATION FILLS A CURRENT GAP IN THE EXISTING CAD LITERATURE EACH CHAPTER CONTAINS ESSENTIAL INFORMATION TO STUDY A TOPIC AT A GREAT DEPTH AND TO UNDERSTAND FURTHER DEVELOPMENTS IN THE FIELD THE BOOK IS INTENDED FOR SENIORS GRADUATE STUDENTS RESEARCHERS AND DEVELOPERS OF RELATED COMPUTER AIDED DESIGN CAD TOOLS FROM THE FOREWORD THE COMMERCIAL SUCCESS OF LOGIC SYNTHESIS AND VERIFICATION IS DUE IN LARGE PART TO THE IDEAS OF MANY OF THE AUTHORS OF THIS BOOK THEIR INNOVATIVE WORK CONTRIBUTED TO DESIGN AUTOMATION TOOLS THAT PERMANENTLY CHANGED THE COURSE OF ELECTRONIC DESIGN BY AART J DE GEUS CHAIRMAN AND CEO SYNOPSYS INC

U-M Computing News

2023-09-14

THIS BOOK PROVIDES THE FOUNDATIONS FOR UNDERSTANDING HARDWARE SECURITY AND TRUST WHICH HAVE BECOME MAJOR CONCERNS FOR NATIONAL SECURITY OVER THE PAST DECADE COVERAGE INCLUDES SECURITY AND TRUST ISSUES IN ALL TYPES OF ELECTRONIC DEVICES AND SYSTEMS SUCH AS ASICS COTS FPGAS MICROPROCESSORS DSPS AND EMBEDDED SYSTEMS THIS SERVES AS AN INVALUABLE REFERENCE TO THE STATE OF THE ART RESEARCH THAT IS OF CRITICAL SIGNIFICANCE TO THE SECURITY OF AND TRUST IN MODERN SOCIETY S MICROELECTRONIC SUPPORTED INFRASTRUCTURES

Embedded System Design

2003

A TEXTBOOK ON THE FUNDAMENTALS OF VLSI DESIGN FLOW COVERING THE VARIOUS STAGES OF DESIGN IMPLEMENTATION VERIFICATION AND TESTING

The Compacts of Free Association and legislative hearing on H.R. 2408, H.R. 3407 and H.R. 4938

2010-04-07

PRESENTING A COMPREHENSIVE OVERVIEW OF THE DESIGN AUTOMATION ALGORITHMS TOOLS AND METHODOLOGIES USED TO DESIGN INTEGRATED CIRCUITS THE ELECTRONIC DESIGN AUTOMATION FOR INTEGRATED CIRCUITS HANDBOOK IS AVAILABLE IN TWO VOLUMES THE SECOND VOLUME EDA FOR IC IMPLEMENTATION CIRCUIT DESIGN AND PROCESS TECHNOLOGY THOROUGHLY EXAMINES REAL TIME LOGIC TO GDSII A FILE FORMAT USED TO TRANSFER DATA OF SEMICONDUCTOR PHYSICAL LAYOUT ANALOG MIXED SIGNAL DESIGN PHYSICAL VERIFICATION AND TECHNOLOGY CAD TCAD CHAPTERS CONTRIBUTED BY LEADING EXPERTS AUTHORITATIVELY DISCUSS DESIGN FOR MANUFACTURABILITY AT THE NANOSCALE POWER SUPPLY NETWORK DESIGN AND ANALYSIS DESIGN MODELING AND MUCH MORE SAVE ON THE COMPLETE SET

The Gospel of the Flying Spaghetti Monster

2012-12-06

THIS BOOK IS ABOUT SECURITY IN EMBEDDED SYSTEMS AND IT PROVIDES AN AUTHORITATIVE REFERENCE TO ALL ASPECTS OF SECURITY IN SYSTEM ON CHIP SOC DESIGNS THE AUTHORS DISCUSS ISSUES RANGING FROM SECURITY REQUIREMENTS IN SOC DESIGNS DEFINITION OF ARCHITECTURES AND DESIGN CHOICES TO ENFORCE AND VALIDATE SECURITY POLICIES AND TRADE OFFS AND CONFLICTS INVOLVING SECURITY FUNCTIONALITY AND DEBUG REQUIREMENTS COVERAGE ALSO INCLUDES CASE STUDIES FROM THE TRENCHES OF CURRENT INDUSTRIAL PRACTICE IN DESIGN IMPLEMENTATION AND VALIDATION OF SECURITY CRITICAL EMBEDDED SYSTEMS PROVIDES AN AUTHORITATIVE REFERENCE AND SUMMARY OF THE CURRENT STATE OF THE ART IN SECURITY FOR EMBEDDED SYSTEMS HARDWARE IPS AND SOC DESIGNS TAKES A CROSS CUTTING VIEW OF SECURITY THAT INTERACTS WITH DIFFERENT DESIGN AND VALIDATION COMPONENTS SUCH AS ARCHITECTURE IMPLEMENTATION VERIFICATION AND DEBUG EACH ENFORCING UNIQUE TRADE OFFS INCLUDES HIGH LEVEL OVERVIEW DETAILED ANALYSIS ON IMPLEMENTATION AND RELEVANT CASE STUDIES ON DESIGN VERIFICATION DEBUG ISSUES RELATED TO IP SOC SECURITY

Logic Synthesis and Verification

2011-09-22

THE SECOND OF TWO VOLUMES IN THE ELECTRONIC DESIGN AUTOMATION FOR INTEGRATED CIRCUITS HANDBOOK SECOND EDITION ELECTRONIC DESIGN AUTOMATION FOR IC IMPLEMENTATION CIRCUIT DESIGN AND PROCESS TECHNOLOGY THOROUGHLY EXAMINES REAL TIME LOGIC RTL TO GDSII A FILE FORMAT USED TO TRANSFER DATA OF SEMICONDUCTOR PHYSICAL LAYOUT DESIGN FLOW ANALOG MIXED SIGNAL DESIGN PHYSICAL VERIFICATION AND TECHNOLOGY COMPUTER AIDED DESIGN TCAD CHAPTERS CONTRIBUTED BY LEADING EXPERTS AUTHORITATIVELY DISCUSS DESIGN FOR MANUFACTURABILITY DFM AT THE NANOSCALE POWER SUPPLY NETWORK DESIGN AND ANALYSIS DESIGN MODELING AND MUCH MORE NEW TO THIS EDITION MAJOR UPDATES APPEARING IN THE INITIAL PHASES OF THE DESIGN FLOW WHERE THE LEVEL OF ABSTRACTION KEEPS RISING TO SUPPORT MORE FUNCTIONALITY WITH LOWER NON RECURRING ENGINEERING NRE COSTS SIGNIFICANT REVISIONS REFLECTED IN THE FINAL PHASES OF THE DESIGN FLOW WHERE THE COMPLEXITY DUE TO SMALLER AND SMALLER GEOMETRIES IS COMPOUNDED BY THE SLOW PROGRESS OF SHORTER WAVELENGTH LITHOGRAPHY NEW COVERAGE OF CUTTING EDGE APPLICATIONS AND APPROACHES REALIZED IN THE DECADE SINCE PUBLICATION OF THE PREVIOUS EDITION THESE ARE ILLUSTRATED BY NEW CHAPTERS ON 3D CIRCUIT INTEGRATION AND CLOCK DESIGN OFFERING IMPROVED DEPTH AND MODERNITY ELECTRONIC DESIGN AUTOMATION FOR IC IMPLEMENTATION CIRCUIT DESIGN AND PROCESS TECHNOLOGY PROVIDES A VALUABLE STATE OF THE ART REFERENCE FOR ELECTRONIC DESIGN AUTOMATION EDA STUDENTS RESEARCHERS AND PROFESSIONALS

Introduction to Hardware Security and Trust

2023-06-15

this book provides a comprehensive and up to date guide to the design of security hardened hardware intellectual property ip readers will learn how ip can be threatened as well as protected by using means such as hardware obfuscation camouflaging watermarking fingerprinting puf functional locking remote activation hidden transmission of data hardware trojan detection protection against hardware trojan use of secure element ultra lightweight cryptography and digital rights management this book serves as a single source reference to design space exploration of hardware security and ip protection

Introduction to VLSI Design Flow

2018-10-03

this book provides the foundations for understanding hardware security and trust which have become major concerns for national security over the past decade coverage includes issues related to security and trust in a variety of electronic devices and systems related to the security of hardware firmware and software spanning system applications online transactions and networking services this serves as an invaluable reference to the state of the art research that is of critical significance to the security of and trust in modern society s microelectronic supported infrastructures

EDA for IC Implementation, Circuit Design, and Process Technology

2017-01-24

this comprehensive text describes the origins mechanisms beneficial applications and practical details of frequency specific therapy a treatment technique that uses frequencies micro amperage current and the principles of biological resonance to treat pain and a wide range of medical conditions it includes condition specific frequency protocols for the treatment of various pain complaints and multi center clinical case reports documenting successful application of the technique each section includes a review of condition pathophysiology and differential diagnosis plus current research a dvd feature a lecture from the author powerpoint teaching slides practical demonstrations of techniques fully searchable text and downloadable images from the book

Fundamentals of IP and SoC Security

2017-02-03

this book demonstrates the breadth and depth of ip protection through logic locking considering both attacker adversary and defender designer perspectives the authors draw a semi chronological picture of the evolution of logic locking during the last decade gathering and describing all the do s and don ts in this approach they describe simple to follow scenarios and guide readers to navigate identify threat models and design evaluation flow for further studies readers will gain a comprehensive understanding of all fundamentals of logic locking

Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology

2017-01-10

the problem of the unknown component theory and applications addresses the issue of designing a component that combined with a known part of a system conforms to an overall specification the authors tackle this problem by solving abstract equations over a language the most general solutions are studied when both synchronous and parallel composition operators are used the abstract equations are specialized to languages associated with important classes of automata used for modeling systems the book is a blend of theory and practice which includes a description of a software package with applications to sequential synthesis of finite state machines specific topologies interconnecting the components exact and heuristic techniques and optimization scenarios are studied finally the scope is enlarged to domains like testing supervisory control game theory and synthesis for special omega languages the authors present original results of the authors along with an overview of existing ones

Foundations of Hardware IP Protection

2015-09-17

the main objective of this workshop was to review and discuss the state of the art and the latest advances in the area of 1 10 gbit s throughput for local and metropolitan area networks the first generation of local area networks had

THROUGHPUTS IN THE RANGE 1 20 MBIT S WELL KNOWN EXAMPLES OF THIS FIRST GENERATION NETWORKS ARE THE ETHERNET AND THE TOKEN RING THE SECOND GENERATION OF NETWORKS ALLOWED THROUGHPUTS IN THE RANGE 100 200 MBIT S REPRESENTATIVES OF THIS GENERATION ARE THE FDDI DOUBLE RING AND THE DQDB IEEE 802 6 NETWORKS THE THIRD GENERATION NETWORKS WILL HAVE THROUGHPUTS IN THE RANGE 1 10 GBIT S THE RAPID DEVELOPMENT AND DEPLOYMENT OF FIBER OPTICS WORLDWIDE AS WELL AS THE PROJECTED EMERGENCE OF A MARKET FOR BROADBAND SERVICES HAVE GIVEN RISE TO THE DEVELOPMENT OF BROADBAND ISDN STANDARDS CURRENTLY THE ASYNCHRONOUS TRANSFER MODE ATM APPEARS TO BE A VIABLE SOLUTION TO BROADBAND NETWORKS THE POSSIBILITY OF ALL OPTICAL NETWORKS IN THE FUTURE IS BEING EXAMINED THIS WOULD ALLOW THE TAPPING OF APPROXIMATELY 50 TERAHERTZ OR SO AVAILABLE IN THE LIGHTWAVE RANGE OF THE FREQUENCY SPECTRUM IT IS ENVISAGED THAT USING SUCH A HIGH SPEED NETWORK IT WILL BE FEASIBLE TO DISTRIBUTE HIGH QUALITY VIDEO TO THE HOME TO CARRY OUT RAPID RETRIEVAL OF RADIOLOGICAL AND OTHER SCIENTIFIC IMAGES AND TO ENABLE MULTI MEDIA CONFERENCING BETWEEN VARIOUS PARTIES

Secure System Design and Trustable Computing

2011-10-28

THIS BOOK CONSTITUTES THE REFEREED PROCEEDINGS OF THE 12TH INTERNATIONAL CONFERENCE ON FIELD PROGRAMMABLE LOGIC AND APPLICATIONS FPL 2002 HELD IN MONTPELLIER FRANCE IN SEPTEMBER 2002 THE 104 REVISED REGULAR PAPERS AND 27 POSTER PAPERS PRESENTED TOGETHER WITH THREE INVITED CONTRIBUTIONS WERE CAREFULLY REVIEWED AND SELECTED FROM 214 SUBMISSIONS THE PAPERS ARE ORGANIZED IN TOPICAL SECTIONS ON RAPID PROTOTYPING FPGA SYNTHESIS CUSTOM COMPUTING ENGINES DSP APPLICATIONS RECONFIGURABLE FABRICS DYNAMIC RECONFIGURATION ROUTING AND PLACEMENT POWER ESTIMATION SYNTHESIS ISSUES COMMUNICATION APPLICATIONS NEW TECHNOLOGIES RECONFIGURABLE ARCHITECTURES MULTIMEDIA APPLICATIONS FPGA BASED ARITHMETIC RECONFIGURABLE PROCESSORS TESTING AND FAULT TOLERANCE CRYPTO APPLICATIONS MULTITASKING COMPILATION TECHNIQUES ETC

Frequency Specific Microcurrent in Pain Management E-book

2023-10-24

THIS SURVEY CONTAINS EXPANDED AND PEER REVIEWED PAPERS BASED ON THE SELECTED CONTRIBUTIONS TO THE WORKSHOP ON ARCHITECTING DEPENDABLE SYSTEMS WADS 2007 AND THE THIRD WORKSHOP ON THE ROLE OF SOFTWARE ARCHITECTURE FOR TESTING AND ANALYSIS ROSATEA 2007

Understanding Logic Locking

2011-11-16

THIS BOOK CONSTITUTES REVISED SELECTED PAPERS FROM THE WORKSHOPSCOLLOCATED WITH THE SEFM 2015 CONFERENCE ON SOFTWARE ENGINEERING ANDFORMAL METHODS HELD IN YORK UK IN SEPTEMBER 2015 THE 25 PAPERS INCLUDED IN THIS VOLUME WERE CAREFULLY REVIEWED AND SELECTED FROM 32 SUBMISSIONS THE SATELLITE WORKSHOPS PROVIDED A HIGHLY INTERACTIVE AND COLLABORATIVE ENVIRONMENT FOR RESEARCHERS AND PRACTITIONERS FROM INDUSTRY AND ACADEMIA TO DISCUSS EMERGING AREAS OF SOFTWARE ENGINEERING AND FORMAL METHODS THE FOUR WORKSHOPS WERE ATSE 2015 THE 6TH WORKSHOP ON AUTOMATING TEST CASE DESIGN SELECTION AND EVALUATION HOFM 2015 THE 2ND HUMAN ORIENTED FORMAL METHODS WORKSHOP MOKMASD 2015 THE 4TH INTERNATIONAL SYMPOSIUM ON MODELLING AND KNOWLEDGE MANAGEMENT APPLICATIONS SYSTEMS AND DOMAINS VERY SCART 2015 THE 1ST INTERNATIONAL WORKSHOP ON THE ART OF SERVICE COMPOSITION AND FORMAL VERIFICATION FOR SELF SYSTEMS

The Unknown Component Problem

2012-12-06

THIS BOOK CONSTITUTES THE REFEREED PROCEEDINGS OF THE 12TH IFIP WG 10 5 ADVANCED RESEARCH WORKING CONFERENCE ON CORRECT HARDWARE DESIGN AND VERIFICATION METHODS CHARME 2003 HELD IN L AQUILA ITALY IN OCTOBER 2003 THE 24 REVISED FULL PAPERS AND 8 SHORT PAPERS PRESENTED WERE CAREFULLY REVIEWED AND SELECTED FROM 65 SUBMISSIONS THE PAPERS ARE ORGANIZED IN TOPICAL SECTIONS ON SOFTWARE VERIFICATION AUTOMATA BASED METHODS PROCESSOR VERIFICATION SPECIFICATION METHODS THEOREM PROVING BOUNDED MODEL CHECKING AND MODEL CHECKING AND APPLICATIONS

High-Capacity Local and Metropolitan Area Networks

2003-08-02

SINCE THE SECOND HALF OF THE 1980S ASYNCHRONOUS CIRCUITS HAVE BEEN THE SUBJECT OF A GREAT DEAL OF RESEARCH FOLLOWING A PERIOD OF RELATIVE OBLIVION THE LACK OF INTEREST IN ASYNCHRONOUS TECHNIQUES WAS MOTIVATED BY THE PROGRESSIVE SHIFT TOWARDS SYNCHRONOUS DESIGN TECHNIQUES THAT HAD MUCH MORE STRUCTURE AND WERE MUCH EASIER TO VERIFY AND SYNTHESIZE SYSTEM DESIGN REQUIREMENTS MADE IT IMPOSSIBLE TO ELIMINATE TOTALLY THE USE OF ASYNCHRONOUS CIRCUITS GIVEN THE OBJECTIVE DIFFICULTY ENCOUNTERED BY DESIGNERS THE ASYNCHRONOUS COMPONENTS OF ELECTRONIC SYSTEMS SUCH AS INTERFACES BECAME A SERIOUS BOTTLENECK IN THE DESIGN PROCESS THE USE OF NEW MODELS AND SOME THEORETICAL BREAKTHROUGHS MADE IT POSSIBLE TO DEVELOP ASYNCHRONOUS DESIGN TECHNIQUES THAT WERE RELIABLE AND EFFECTIVE THIS BOOK DESCRIBES A VARIETY OF MATHEMATICAL MODELS AND OF ALGORITHMS THAT FORM THE BACKBONE AND THE BODY OF A NEW DESIGN METHODOLOGY FOR ASYN CHRONOUS DESIGN THE BOOK IS INTENDED FOR ASYNCHRONOUS HARDWARE DESIGNERS FOR COMPUTER AIDED TOOL EXPERTS AND FOR DIGITAL DESIGNERS INTERESTED IN EX PLORING THE POSSIBILITY OF DESIGNING ASYNCHRONOUS CIRCUITS IT REQUIRES A SOLID MATHEMATICAL BACKGROUND IN DISCRETE EVENT SYSTEMS AND

ALGORITHMS WHILE THE BOOK HAS NOT BEEN WRITTEN AS A TEXTBOOK NEVERTHELESS IT COULD BE USED AS A REFERENCE BOOK IN AN ADVANCED COURSE IN LOGIC SYNTHESIS OR ASYNCHRONOUS DESIGN

Field-Programmable Logic and Applications: Reconfigurable Computing Is Going Mainstream

2008-08-28

CHIP DESIGN AND IMPLEMENTATION FROM A PRACTICAL VIEWPOINT FOCUSING ON CHIP IMPLEMENTATION LOW POWER NOC FOR HIGH PERFORMANCE SOC DESIGN PROVIDES PRACTICAL KNOWLEDGE AND REAL EXAMPLES OF HOW TO USE NETWORK ON CHIP NOC IN THE DESIGN OF SYSTEM ON CHIP SOC IT DISCUSSES MANY ARCHITECTURAL AND THEORETICAL STUDIES ON NOCS INCLUDING DESIGN METHODOLOGY TOPOLOGY EXPLORATION QUALITY OF SERVICE GUARANTEE LOW POWER DESIGN AND IMPLEMENTATION TRIALS THE STEPS TO IMPLEMENT NOC THE BOOK COVERS THE FULL SPECTRUM OF THE SUBJECT FROM THEORY TO ACTUAL CHIP DESIGN USING NOC EMPLOYING THE UNIFIED MODELING LANGUAGE UML THROUGHOUT IT PRESENTS COMPLICATED CONCEPTS SUCH AS MODELS OF COMPUTATION AND COMMUNICATION COMPUTATION PARTITIONING IN A MANNER ACCESSIBLE TO LAYPEOPLE THE AUTHORS PROVIDE GUIDELINES ON HOW TO SIMPLIFY COMPLEX NETWORKING THEORY TO DESIGN A WORKING CHIP IN ADDITION THEY EXPLORE THE NOVEL NOC TECHNIQUES AND IMPLEMENTATIONS OF THE BASIC ON CHIP NETWORK BONE PROJECT EXAMPLES OF REAL TIME DECISIONS CIRCUIT LEVEL DESIGN SYSTEMS AND CHIPS GIVE THE MATERIAL A REAL WORLD CONTEXT LOW POWER NOC AND ITS APPLICATION TO SOC DESIGN EMPHASIZING THE APPLICATION OF NOC TO SOC DESIGN THIS BOOK SHOWS HOW TO BUILD THE COMPLICATED INTERCONNECTIONS ON SOC WHILE KEEPING A LOW POWER CONSUMPTION

Architecting Dependable Systems V

2023-04-10

THIS BOOK CONSTITUTES THE PROCEEDINGS OF THREE INTERNATIONAL CONFERENCES NECOM 2011 ON NETWORKS COMMUNICATIONS WEST 2011 ON AND SEMANTIC TECHNOLOGY AND WIMON 2011 ON WIRELESS AND MOBILE NETWORKS JOINTLY HELD IN CHENNAI INDIA IN JULY 2011 THE 74 REVISED FULL PAPERS PRESENTED WERE CAREFULLY REVIEWED AND SELECTED FROM NUMEROUS SUBMISSIONS THE PAPERS ADDRESS ALL TECHNICAL AND PRACTICAL ASPECTS OF NETWORKS AND COMMUNICATIONS IN WIRELESS AND MOBILE NETWORKS DEALING WITH ISSUES SUCH AS NETWORK PROTOCOLS AND WIRELESS NETWORKS DATA COMMUNICATION TECHNOLOGIES AND NETWORK SECURITY THEY PRESENT KNOWLEDGE AND RESULTS IN THEORY METHODOLOGY AND APPLICATIONS OF THE AND SEMANTIC TECHNOLOGIES AS WELL AS CURRENT RESEARCH ON WIRELESS AND MOBILE COMMUNICATIONS NETWORKS PROTOCOLS AND ON WIRELESS AND MOBILE SECURITY

Advanced Modeling and Simulation of Nuclear Reactors

2016-01-11

THE DESIGNER OF A SOFTWARE SYSTEM LIKE THE ARCHITECT OF A BUILDING NEEDS TO BE AWARE OF THE CONSTRUCTION TECHNIQUES AVAILABLE AND TO CHOOSE THE ONES THAT ARE THE MOST APPROPRIATE THIS BOOK PROVIDES THE IMPLEMENTER OF SOFTWARE SYSTEMS WITH A GUIDE TO 25 DIFFERENT TECHNIQUES FOR THE COMPLETE DEVELOPMENT PROCESSES FROM SYSTEM DEFINITION THROUGH DESIGN AND INTO PRODUCTION THE TECHNIQUES ARE DESCRIBED AGAINST A COMMON BACKGROUND OF THE TRADITIONAL DEVELOPMENT PATH ITS ACTIVITIES AND DELIVERABLE ITEMS IN ADDITION THE CONCEPTS OF METRICS AND INDICATORS ARE INTRODUCED AS TOOLS FOR BOTH TECHNICAL AND MANAGERIAL MONITORING AND CONTROL OF PROGRESS AND QUALITY THE BOOK IS INTENDED TO WIDEN THE MENTAL TOOLKIT OF SYSTEM DEVELOPERS AND THEIR MANAGERS AND WILL ALSO INTRODUCE STUDENTS OF COMPUTER SCIENCE TO THE PRACTICAL SIDE OF SOFTWARE DEVELOPMENT WITH ITS WIDE RANGING TREATMENT OF THE TECHNIQUES AVAILABLE AND THE PRACTICAL GUIDANCE IT OFFERS IT WILL PROVE AN IMPORTANT AND VALUABLE WORK

Software Engineering and Formal Methods

2003-10-10

THIS BOOK CONSTITUTES THE REFEREED PROCEEDINGS OF THE 13TH INTERNATIONAL WORKSHOP ON POWER AND TIMING MODELING OPTIMIZATION AND SIMULATION PATMOS 2003 HELD IN TORINO ITALY IN SEPTEMBER 2003 THE 43 REVISED FULL PAPERS AND 18 REVISED POSTER PAPERS PRESENTED TOGETHER WITH THREE KEYNOTE CONTRIBUTIONS WERE CAREFULLY REVIEWED AND SELECTED FROM 85 SUBMISSIONS THE PAPERS ARE ORGANIZED IN TOPICAL SECTIONS ON GATE LEVEL MODELING AND CHARACTERIZATION INTERCONNECT MODELING AND OPTIMIZATION ASYNCHRONOUS TECHNIQUES RTL POWER MODELING AND MEMORY OPTIMIZATION HIGH LEVEL MODELING POWER EFFICIENT TECHNOLOGIES AND DESIGNS COMMUNICATION MODELING AND DESIGN AND LOW POWER ISSUES IN PROCESSORS AND MULTIMEDIA

Correct Hardware Design and Verification Methods

2012-12-06

THE COMPACT OF FREE ASSOCIATION BETWEEN THE REPUBLIC OF PALAU AND THE U S ENTERED INTO FORCE ON OCT 1 1994 WITH THE U S INTEREST OF PROMOTING PALAU S SELF SUFFICIENCY AND ECONOMIC ADVANCEMENT THE COMPACT AND ITS RELATED SUBSIDIARY AGREEMENTS PROVIDE FOR A 15 YEAR TERM OF ECONOMIC ASSISTANCE IN FY 2009 THE TWO GOVERNMENTS MUST REVIEW THE TERMS OF THE COMPACT AND RELATED AGREEMENTS AND AGREE ON ANY MODIFICATIONS THIS IS A REPORT ON 1 THE PROVISION OF COMPACT AND OTHER U S ASSISTANCE TO PALAU IN FY 1995 2009 2 PALAU S AND U S AGENCIES EFFORTS TO PROVIDE ACCOUNTABILITY OVER PALAU S USE OF FED FUNDS IN 1995 2006 AND 3 PALAU S PROSPECTS FOR ACHIEVING ECONOMIC SELF SUFFICIENCY INCLUDES RECOMMENDATIONS ILLUS

Algorithms for Synthesis and Testing of Asynchronous Circuits

2018-10-08

this book constitutes the refereed proceedings of the 16th international conference on product focused software process improvement profes 2015 held in bolzano italy in december 2015 the 18 revised full papers presented together with 10 short papers and 18 workshop papers were carefully reviewed and selected from 50 submissions the papers are organized in topical sections on lessons learned from industry research collaborations instruments to improve the software development process requirements features and release management practices of modern development processes human factors in modern software development effort and size estimation validated by professionals empirical generalization software reliability and testing in industry workshop on processes methods and tools for engineering embedded systems workshop on human factors in software development processes and workshop on software startups state of the art and state of the practice

Low-Power NoC for High-Performance SoC Design

2011-06-30

the past few years have seen a rapid growth in image processing and image communication technologies new video services and multimedia applications are continuously being designed essential for all these applications are image and video compression techniques the purpose of this book is to report on recent advances in vlsi architectures and their implementation for video signal processing applications with emphasis on video coding for bit rate reduction efficient vlsi implementation for video signal processing spans a broad range of disciplines involving algorithms architectures circuits and systems recent progress in vlsi architectures and implementations has resulted in the reduction in cost and size of video signal processing equipment and has made video applications more practical the topics covered in this volume demonstrate the increasingly interdisciplinary nature of vlsi implementation of video signal processing applications involving interactions between algorithms vlsi architectures circuit techniques semiconductor technologies and cad for microelectronics

Trends in Network and Communications

1988-02-11

this book provides an overview of emerging topics in the field of hardware security such as artificial intelligence and quantum computing and highlights how these technologies can be leveraged to secure hardware and assure electronics supply chains the authors are experts in emerging technologies traditional hardware design and hardware security and trust readers will gain a comprehensive understanding of hardware security problems and how to overcome them through an efficient combination of conventional approaches and emerging technologies enabling them to design secure reliable and trustworthy hardware

A Practical Handbook for Software Development

2003-09-03

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation

2009-02

Compact of Free Association

2015-11-28

Product-Focused Software Process Improvement

2014-06-28

VLSI Implementations for Image Communications

2021-04-30

Emerging Topics in Hardware Security

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